International Journal of Research in Advent Technology, Vol.2, No.5, May 2014
E-ISSN: 2321-9637

VLSI Implementation of High Speed DCT Architecture for H.264 Video Codec Design

Devachandran D, Lavanya V, Vinoth kumar S
M.E., Applied Electronics, Asst. Professor, Dept. of ECE, HOD,Dept of ECE
Aksheyaa College of Engineering
devachand1@gmail.com, lavanyaruban06@gmail.com, aceece12@gmail.com

Abstract: Field programmable gate arrays are ideally suited for the implementation of DCT based digital image compression. However, there are several issues that need to be solved. The Multiply-Accumulate Unit (MAC) is the main computational kernel in DIP architectures. The MAC unit establishes the power and the speed of the overall system; it always lies in the critical path. To develop high speed and low power MAC is crucial to use DSP in the future wireless sensor networks. In this work, a fast and low power MAC Unit is proposed for 2D-DCT computation. The proposed architecture is based on modified booth radix-8 with merged MAC architectures to design a unit with a low critical path delay and low hardware complexity. This new architecture reduces the hardware complexity of the summation network to reduce the overall power and area. Increasing the speed of operation is achieved by feeding the bits of the accumulated operand into the summation tree before the final adder instead of going through the entire summation network. The FPGA implementation of the proposed booth radix-8 based MAC unit saves 64% of the area, to the regular merged MAC unit with conventional multiplier.

Keywords: *Discrete cosine transform(DCT),very large scale integration (VLSI), Digital signal processing (*DSP*).*

1. INTRODUCTION

The applications of the digital images are more and more extensive today than ever before. In recent years, the design for high speed with low power consumption has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to reduce the power consumption with high performance of new VLSI systems. However, most of these methods focus on the power consumption and quality enhancement by replacing multipliers with distribute arithmetic approach [1]-[2]. But this increase the overall delay makes them unsuitable for high speed applications.

In the last decade many research have been carried out to reduce the computation complexity, and quality enhancement of DCT. Most of them are efficient with software implementation, but unfortunately due to their irregular structure and complex routing, these algorithms are not suitable for VLSI implementation. Our goal is to design a high speed 8x8 DCT chip suitable for the application in HDTV system. To reduce the area of the circuit, the fixed-width multipliers will be only kept the most significant half part of the products. It will lead large error, many compensation methods are used to solve this problem [3]-[4].

Here we attempt to increase the speed of multiplication by reducing number of partial products generated using high radix booth algorithm and combine it with partial addition of partial product addition using truncation technique. The main concerns are speed and error compensation in DCT computation.

2. FPGA IMPLEMENTATION

Field programmable gate arrays were actually invented only for prototyping the digital design which is later to be used in IC's. But in recent days FPGA's are started to use as a product in many fields. So Field programmable gate arrays are ideally suited for the implementation of DCT based digital image compression. However, there are several issues that need to be solved. When performing software simulation of DCT, calculations are carried out with floating point precision. But in FPGA resources available to perform floating point arithmetic is unjustified, and measures to be taken to account for this. Another concern is the DCT coefficients value itself. Many techniques have been used to efficiently convert this floating point values into binary representation for digital implementation. Then only we can implement DCT in VLSI.

The two ways of floating point to binary conversion are

1. Both integral and fractional part is converted separately by repeatedly multiply 2, and considers each one bit as it appears left of the decimal.
2. Representing the floating number using IEEE 754 format (single or double precision).

Method 1 can be used efficiently if we use any shift and add based approach for DCT computation.

For method 2 we need to have floating point arithmetic unit for computation.

3. BOOTH MULTIPLIER

In the modern world, we need system which will run at high speed. Multipliers play an important part in today's DSP and DIP applications. In our case for DCT computation multiplications are used larger in number. Therefore, speed improvement in multiplier is important. Advances in technology have permitted many researchers to design multipliers which offer both high-speed and unique hardware structure, thereby making them suitable for specific VLSI implementation.

In any multiplication algorithm, the multiplication operation is carried out by summation of decomposed partial products. For high-speed multiplication we need to apply a booth radix recoding multiplication algorithm. In recent days in all high radix booth algorithm recoding is changed from 2s-complement format to a signed-digit representation from the defined set. This is called modified booth algorithm..

3.1 Radix-8 Algorithm

Here we reduce the number of partial products using a higher radix in the multiplier recoding. Recoding of binary numbers was first invented by Booth [5]. The modified Booth's algorithm is done by appending a zero to the right of M. Figure 2 shows recoding of $0101000102_{.}$ In radix-8 recoding is similar to radix-4 [6] but here we take four bits instead of three bits and then we represent that coded values in signed-digit representation using TABLE I.

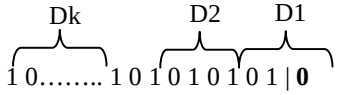

Fig 2: Recoding representation

Where *k* is the number of partial products to be generated.

3.2 Preprocessing Stage.

Both 2N and 4N is achieved by simple left shift of N. and 3N is calculated by adding 2N and N. If the bit width of N is high this will increase the delay in preprocessing stage. After this stage only we can generate partial products. In order to reduce the delay here we use Carry select adder. The resource used in CSA adder later will be used for partial product addition.

TABLE I. Radix-8 sign digit values

Coded bits	signed-digit value
0000	0
0001	+1
0010	+1
0011	+2
0100	+2
0101	+3
0110	+3
0111	+4
1000	-4
1001	-3
1010	-3
1011	-2
1100	-2
1101	-1
1110	-1
1111	0

From the TABLE I we need to have 2N, 3N, 4N and its 2's complement respectively.

3.3 Wallace Tree

As we discuss in section 1 truncation errors will occur when we remove least significant bits from multiplied result. Here we use Wallace array to represent partial products array and its summation, which gives the multiplication result. First four partial products are processed using 4-2 compressor which is made up of two full adders. In later stages we used only Full adder for partial product addition.

In radix-8 partial products are left shifted by three bits. So in partial products some of the LSB bits will become 0's. It is predefined one. So these bits are not considered here in Wallace tree structure in order to save the hardware resource. In Wallace tree partial products are divided into main part and truncation part. Resource used in truncation part is reconfigured based on number of columns need to be selected for error compensation.

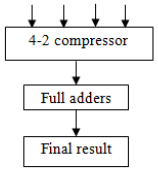

Fig 3: Wallace tree structure

4. PERFORMANCE ANALYSIS

The image is converted into blocks using MATLAB and the values are stored as a text file. The text file is accessed by the Modelsim and the corresponding 2-D DCT coefficients are calculated. These values are then fed to the 2-D IDCT module which returns the data sequence. These data are written to a text file. The image can be reconstructed from the text file using MATLAB coding.

TABLE II
COMPARISON OF PARAMETRS

Parameters	Conventional method	Proposed booth multiplier
AREA	349	213

5. CONCLUSION

We propose a unique high speed booth multiplier based MAC unit to improve throughput rate and to minimize the area complexity of 8x8 2D DCT architecture. In the DCT architecture, DCT computation is performed with sufficiently high precision in DCT matrix multiplication yielding an acceptable quality. Our proposed MAC architecture achieves a maximum operating frequency of 129.18MHz MHz .In summary the proposed architecture is suitable for applications in HDTV system.

REFERENCES

[1] S. Yu and E. E. S. ,Jr., "DCT implementation with distributed arithmetic*"IEEE Trans. Comput.*, vol. 50, no. 9, pp. 985–991, Sep. 2001.

[2] P. K. Meher, "Unified systolic-like architecture for DCT and DST using distributed arithmetic," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 12, pp. 2656–2663, Dec. 2006.

[3] L. D. Van and C. C. Yang, "Generalized low-error area-efficient fixedwidth multipliers," IEEE Trans. Circuits Syst. I, vol. 52, no. 8, pp. 1608– 1619, Aug. 2005.

[4] C. H. Chang and R. K. Satzoda, "A low error and high performance multiplexer-based truncated multiplier," IEEE Trans. VLSI Syst., vol. 18, no. 12, pp. 1767–1771, Dec. 2010.

[5] C. Lu, S. P. A.D. Booth, "A signed binary multiplication technique," Quarterly J. Mechan. Appl. Math., vol IV. Part 2, 1951.

[6] Yuan-Ho Chen and Hsin-Chen Chiang "Modified Booth Encoding Radix-4 8-bit Multiplier" .2012

[7] Prasad, K,"Low-power 4-2 and 5-2 compressors" vol. 1, pp. 129 – 133, Nov. 2001.

[8] Jongsun Park · Kaushik Roy "A Low Complexity Reconfigurable DCT Architecture to Trade off Image Quality for Power Consumption", Springer Science Business Media, April 2008.